Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

All claims currently being amended are shown with deleted text struckthrough or double bracketed and new text underlined. Additionally, the status of each claim is indicated in parenthetical expression following the claim number.

Claims 2-6, 8-13, and 15-20 remain.

Claims 2-6, 8-13, and 15-20 are being amended.

Claims 1, 7, and 14 are being cancelled.

Claims 21-26 are being added.

WHAT IS CLAIMED IS:

1. Cancelled.

2. (Currently Amended) The pulse width modulator of Claim 4 [[1]], wherein the pulse width modulation circuitry comprises a pulse width modulation encoder and another parallel pulse width modulation encoder for generating the stream and the another stream.

3. (Currently Amended) ~~The pulse width modulator of Claim 2,~~ A pulse width modulator comprising:

at least one input for receiving an input signal, wherein the at least one input comprises an input for receiving a first split of each value of the input signal and another input for receiving a second split of each value of the input signal;

pulse width modulation circuitry including a pulse width modulation encoder for generating a pulse width modulated stream and another parallel pulse width modulation encoder for generating another pulse width modulated stream, the pulse width modulated stream and the another pulse width modulated stream being nominally out of phase and together representing the received input signal; and

a summer for summing the pulse width modulated stream and the another pulse width modulated stream to generate an analog output signal.

4. (Currently Amended) ~~The pulse width modulator of Claim 1,~~ A pulse width modulator comprising:

at least one input for receiving an input signal, wherein the input signal comprises delta-sigma modulated data at [[of]] a selected quantization level;

pulse width modulation circuitry including a pulse width modulation encoder for generating a pulse width modulated stream and another parallel pulse width modulation encoder for generating another pulse width modulated stream, the pulse width modulated stream and the another pulse width modulated stream being nominally out of phase and together representing the received input signal; and

a summer for summing the pulse width modulated stream and the another pulse width modulated stream to generate an analog output signal.

5. (Currently Amended) The pulse width modulator of Claim 4 [[1]], wherein the pulse width modulation circuitry generates the stream and the another stream having equal duty cycles in response to a midlevel value of the input signal.

6. (Currently Amended) The pulse width modulator of Claim 4 [[5]], wherein the pulse width modulation circuitry generates the stream and the another stream with symmetrical waveforms in response to a midlevel value of the input signal.

7. Cancelled.

8. (Currently Amended) ~~The digital to analog converter of Claim 7, further comprising~~ A digital to analog converter comprising:

a pulse width modulation stage for receiving a modulator input stream and outputting in response a duty cycle modulated stream and simultaneously another duty cycle modulated stream, the duty cycle modulated stream and the another duty cycle modulated stream being nominally out of phase;

conversion circuitry for converting the duty cycle modulated stream and the

another duty cycle modulated stream into an analog signal; and

a mismatch shaper for selectively distributing variations in duty cycle between the duty cycle modulated stream and the another duty cycle modulated stream for odd values of the input stream.

9. (Currently Amended) ~~The digital to analog converter of Claim 7,~~ A digital to analog converter comprising:

a pulse width modulation stage for receiving a modulator input stream and outputting in response a duty cycle modulated stream and simultaneously another duty cycle modulated stream, the duty cycle modulated stream and the another duty cycle modulated stream being nominally out of phase; and

conversion circuitry for converting the duty cycle modulated stream and the another duty cycle modulated stream into an analog signal, wherein the conversion circuitry comprises:

a finite impulse response filter for converting the duty cycle modulated stream into a plurality of filtered data streams;

another finite impulse response filter for converting the another duty cycle modulated stream into another plurality of filtered data streams; and

a summer for summing the plurality and the another plurality of filtered data streams into the analog signal.

10. (Original) The digital to analog converter of Claim 9, wherein the plurality and the another plurality of filtered data streams comprise currents of selected weights.

11. (Currently Amended) ~~The digital to analog converter of Claim 7,~~ A digital to analog converter comprising:

a pulse width modulation stage for receiving a modulator input stream and outputting in response a duty cycle modulated stream and simultaneously another duty cycle modulated stream, the duty cycle modulated stream and the another duty cycle modulated stream being nominally out of phase; and

conversion circuitry for converting the duty cycle modulated stream and the

another duty cycle modulated stream into an analog signal; and

~~further comprising~~ a delta-sigma modulator for generating the modulator input stream in response to a received digital stream.

12. (Currently Amended) ~~The digital to analog converter of Claim 7, further comprising:~~ A digital to analog converter comprising:

a pulse width modulation stage for receiving a modulator input stream and outputting in response a duty cycle modulated stream and simultaneously another duty cycle modulated stream, the duty cycle modulated stream and the another duty cycle modulated stream being nominally out of phase;

conversion circuitry for converting the duty cycle modulated stream and the another duty cycle modulated stream into an analog signal,

another pulse width modulation stage for receiving a modulator input stream and outputting in response a duty cycle modulated stream and simultaneously another duty cycle modulated stream to the conversion circuitry; and

interleave circuitry for interleaving the single modulator input stream between inputs to the pulse width modulation stage and the another pulse width modulation stage.

13. (Original) The digital to analog converter of Claim 12, further comprising a delta-sigma modulator for generating the modulator input stream, the delta-sigma modulator having a signal transfer function with multiple attenuation bands.

14. Cancelled.

15. (Currently Amended) The method of Claim 17 [[14]], wherein the first and second duty cycles are substantially equal for a midlevel input value.

16. (Currently Amended) The method of Claim 17 [[14]], wherein the first and second duty cycle modulated pulses have complementary waveforms for a midlevel input value.

17. (Currently Amended) ~~The method of Claim 14, further comprising~~ A method of

duty cycle modulation comprising:

receiving input data representing an input value;

generating first and second nominally out of phase duty cycle modulated pulses having respective first and second duty cycles from the input data, the first and second duty cycles summed to generate an output signal corresponding to the input value; and

noise shaping the input data prior to generating the first and second duty cycle pulses.

18. (Currently Amended) ~~The method of Claim 14, further comprising~~ A method of duty cycle modulation comprising:

receiving input data representing an input value;

generating first and second nominally out of phase duty cycle modulated pulses having respective first and second duty cycles from the input data, the first and second duty cycles summed to generate an output signal corresponding to the input value; and

switching the input data to a selected one of a set of pulse width modulation stages for generating the first and second duty cycle modulated pulses.

19. (Currently Amended) ~~The method of Claim 14, further comprising~~ A method of duty cycle modulation comprising:

receiving input data representing an input value;

generating first and second nominally out of phase duty cycle modulated pulses having respective first and second duty cycles from the input data, the first and second duty cycles summed to generate an output signal corresponding to the input value; and

mismatch shaping by selecting a one of the first and second duty cycles to be varied for an odd input value.

20. (Currently Amended) ~~The method of Claim 14, further comprising~~ A method of duty cycle modulation comprising:

receiving input data representing an input value;

generating first and second nominally out of phase duty cycle modulated pulses having respective first and second duty cycles from the input data, the first and second

duty cycles summed to generate an output signal corresponding to the input value; and

filtering the outputs of the first and second duty cycle modulated streams with first and second finite impulse response filters.

21. (New) The pulse width modulator of Claim 3, wherein the pulse width modulation circuitry generates the stream and the another stream having equal duty cycles in response to a midlevel value of the input signal.

22. (New) The pulse width modulator of Claim 3, wherein the pulse width modulation circuitry generates the stream and the another stream with symmetrical waveforms in response to a midlevel value of the input signal.

23. (New) The digital to analog converter of Claim 8, wherein the conversion circuitry comprises:

a finite impulse response filter for converting the duty cycle modulated stream into a plurality of filtered data streams;

another finite impulse response filter for converting the another duty cycle modulated stream into another plurality of filtered data streams; and

a summer for summing the plurality and the another plurality of filtered data streams into the analog signal.

24. (New) The digital to analog converter of Claim 8, further comprising a delta-sigma modulator for generating the modulator input stream, the delta-sigma modulator having a signal transfer function with multiple attenuation bands.

25. (New) The method of Claim 18, wherein the first and second duty cycles are substantially equal for a midlevel input value.

26. (New) The method of Claim 18, wherein the first and second duty cycle modulated pulses have complementary waveforms for a midlevel input value.